

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application:

**LISTING OF CLAIMS**

**1. – 5. (canceled)**

**6. (original)** A method of confusing a reverse engineer comprising the steps of:  
    providing a false semiconductor device without sidewall spacers having at least one active region; and  
    forming a conductive layer partially over the at least one active region such that an artifact edge of said conductive layer of said false semiconductor device without sidewall spacers mimics an artifact edge of a conductive layer of a semiconductor device having sidewall spacers.

**7. (original)** The method of claim 6 wherein the conductive layer is a silicide layer.

**8. (original)** The method of claim 6 wherein the false semiconductor device is a false transistor having a polysilicon gate and wherein the step of forming a conductive layer comprises the step of modifying a conductive layer block mask such that the artifact edge of said conductive layer is offset from an edge of said polysilicon gate.

**9. (original)** The method of claim 8 wherein the offset between the artifact edge of said conductive layer and said edge of said polysilicon gate is approximately equal to a width of a sidewall spacer.

**10 – 18 (canceled)**